

## CLAIMS

WE CLAIM:

1. A processor unit for a shared-memory computer comprising:  
a processor;  
a local memory system executing a protocol to share data with at least one  
other processor unit;  
5 a conflicts resolution circuit executing a hardware program to:
  - (i) detect a critical section in an executing program and begin  
speculative execution of the critical section without acquisition of a lock;
  - (ii) in the event of a conflict with another processor unit executing the  
critical section and needing to write to data within the critical section,  
10 establishing a priority between the processor units to resolve the conflict  
without acquisition of the lock.
2. The processor unit of claim 1 further including:  
a globally unique clock;  
and where the conflicts resolution circuit establishes a priority between the  
processor units by:  
5
  - (a) time stamping requests for data sent by the given processor unit to  
other processor units with a value of the globally unique clock;
  - (b) releasing owned data requested by a second processor unit  
making a request with an earlier time stamp than a time stamp of a request to  
acquire ownership of the data by the processor unit; and  
10
  - (c) deferring release of owned data requested by a second processor  
unit making a request having a later time stamp than the time stamp of the  
request to acquire ownership of the data by the processor unit.
3. The processor unit of claim 2 wherein the conflicts resolution circuit  
executes hardware program step (i) only during execution of a critical section.

4. The processor unit of claim 2 wherein the conflicts resolution circuit defers to the protocol of the local memory during execution of a section of the program that is not a critical section.

5. The processor unit of claim 4 wherein the protocol of the local memory is a cache coherence protocol.

6. The processor unit of claim 1 wherein the globally unique clock includes a time variant field and a static processor-unit-dependant field.

7. The processor unit of claim 1 wherein the globally unique clock is a counter updated after executions by the processor of a critical section of a program subject to a lock.

8. The processor unit of claim 7 wherein the counter sets itself to a higher number on updating.

9. The processor unit of claim 8 wherein the counter sets itself to the time stamp of the request of the other processor unit when the release of data is deferred because the time stamp of the request of the other processor unit is later.

10. The processor unit of claim 1 further including buffer memory storing the deferred request of the other processor unit; and

wherein the conflicts resolution circuit further executes the hardware program to:

5 (iv) read the buffered deferred requests at a time after the deferring to release data to the other processor unit.

11. The processor unit of claim 10 further including:  
a critical section detection circuit detecting the start and end of execution by the processor of a critical section of a program subject to a lock; and  
wherein the later time is the completion of a critical section.

12. The processor unit of claim 1 wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a marker message to the second processor unit when the request by the second processor unit is deferred based on its time stamp.

13. The processor unit of claim 1 wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a marker message to the second processor unit when the request by the second processor unit is deferred because the requested data is not available.

14. The processor unit of claim 13 wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a probe message to a third processor unit containing a time stamp of the request of a second processor unit receiving the marker message.

15. The processor unit of claim 1 wherein the conflicts resolution circuit further executes the hardware program to:

(iv) respond to a probe message to a second processor unit that has sent the processor unit a marker message indicating that a request by the processor unit has been deferred, the probe message indicating a time stamp of a third processor unit earlier than the time stamp of the request used by processor unit to acquire that data, the probe message being from a third processor unit requesting the data from the second processor unit.

16. The processor unit of claim 1 further including:

a lock elision circuit executing a hardware program to:

(i) detect the start of execution by the processor of a critical section of a program subject to a lock;

(ii) speculatively execute the critical section without acquiring the lock;

(iii) when a conflict for data of the critical section is detected, refer the conflict to the conflict resolution circuit, where the conflict is indicated by a request by another processor unit for data in the critical section owned by the processor unit; and

(iv) when no conflict for data of the critical section is detected, commit the execution of the critical section.

17. The processor unit of claim 16 wherein the conflict resolution circuit allows continued speculative execution of the critical section when the conflict is resolved by deferring the release of the data per hardware program step (iii).

18. The processor unit of claim 16 wherein the conflict resolution circuit causes a ceasing of the speculative execution of the critical section when the conflict is resolved by releasing the data per hardware program step (iii).

19. The processor unit of claim 16 further including buffer memory storing deferred requests from the other processor unit; and

wherein the conflicts resolution circuit further executes the hardware program to:

(iv) read the buffered deferred requests at a later time to release data to the other processor unit; and

(v) cease the speculative execution of the critical section when buffer memory is exhausted.

20. The processor unit of claim 16 including buffer memory storing the results of speculative execution; and

wherein the lock elision circuit further executes the hardware program to:

(iv) cease the speculative execution of the critical section when buffer memory is exhausted.

21. A processor unit system comprising:

a plurality of processor units having:

a processor;

a local memory system executing a protocol to share data with at least one  
5 other processor unit;  
a globally unique clock;  
a conflicts resolution circuit executing a hardware program to:  
(i) time stamp requests for data sent by the given processor unit to  
other processor units with a value of the globally unique clock;  
10 (ii) release owned data requested by a second processor unit making a  
request with an earlier time stamp than a time stamp of a request to acquire  
ownership of the data by the processor unit;  
(iii) defer release of owned data requested by a second processor unit  
making a request having a later time stamp than the time stamp of the request  
15 to acquire ownership of the data by the processor unit.

22. A method of operating a set of processor units for a shared-memory  
computer comprising the steps of:  
(a) generating on each processor unit a globally unique clock;  
(b) time stamping all requests for data sent by the given processor unit to  
5 other processor units with a value of the globally unique clock;  
(c) releasing owned data requested by a second processor unit making a  
request with an earlier time stamp than a time stamp of a request to acquire  
ownership of the data by the processor unit; and  
(d) deferring release of owned data requested by a second processor unit  
10 making a request having a later time stamp than the time stamp of the request to  
acquire ownership of the data by the processor unit.

23. A processor unit for a shared-memory computer comprising:  
a processor;  
a local memory system executing a protocol to share data with at least one  
other processor unit;  
5 a conflicts resolution circuit executing a hardware program to resolve  
conflicts between different processor units;  
a lock elision circuit executing a hardware program to:

(i) detect the start of execution by the processor of a critical section of a program subject to a lock;

10           (ii) speculatively execute the critical section without acquiring the lock;

              (iii) when a conflict for data of the critical section is detected, refer the conflict to the conflict resolution circuit, where the conflict is indicated by a request by another processor unit for data in the critical section owned  
15 by the processor unit; and

              (iv) when no conflict for data of the critical section is detected, commit the execution of the critical section.